N Channel Enhancement

- High speed switching
- Very low switching losses
- Fully controllable dv/dt
- High blocking voltage with low on-resistance
- Fast intrinsic diode with low reverse recovery (Qrr)
- Temperature independent turn-off switching losses
- Halogen free, RoHS compliant

- Cooling effort reduction
- Efficiency improvement
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency

- On-board charger/PFC
- EV battery chargers
- Booster/DC-DC converter
- Switch mode power supplies

(Tc = 25°C unless otherwise specified)

(Tc = 25°C unless otherwise specified)

$V_{(BR)DSS}$	Drain-source breakdown voltage	1200	-	-	V	V_{GS} = 0V, I_D = 100μA	
$V_{GS(th)}$	Gate threshold voltage	2.3	2.8	3.6	V	V_{DS} = V_{GS}, I_D = 9mA	Fig.11
		-	2.2	-	V	V_{DS} = V_{GS}, I_D = 9mA T_J = 175°C	
I_{DSS}	Zero gate voltage drain current	-	1	10	μA	V_{DS} = 1200V, V_{GS} = 0V	
I_{GSS}	Gate source leakage current	-	-	100	nA	V_{GS} = 18V, V_{DS} = 0V	
$R_{DS(on)}$	Current drain-source on-state resistance	-	34	50	mΩ	V_{GS} = 15V, I_D = 32A	Fig.4,5,6
		-	54	-		V_{GS} = 15V, I_D = 32A, T_J = 175°C	
		-	28.5	40		V_{GS} = 18V, I_D = 32A	
		-	51	-		V_{GS} = 18V, I_D = 32A, T_J = 175°C	
g_{fs}	Transconductance	-	24	-	S	V_{DS} = 20V, I_D = 32A	Fig.7
		-	23	-		V_{DS} = 20V, I_D = 32A, T_J = 175°C	
$R_{g,int}$	Intenal gate resistance	-	2.7	-	Ω	V_{AC} = 25mV, f = 1MHz, open drain	

(Tc = 25°C unless otherwise specified)

C_{iss} Input capacitance

Q_{gs}	Gate source charge	-	19	-	nC	V_{DS} = 800V, V_{GS} = -4/+18V I_D

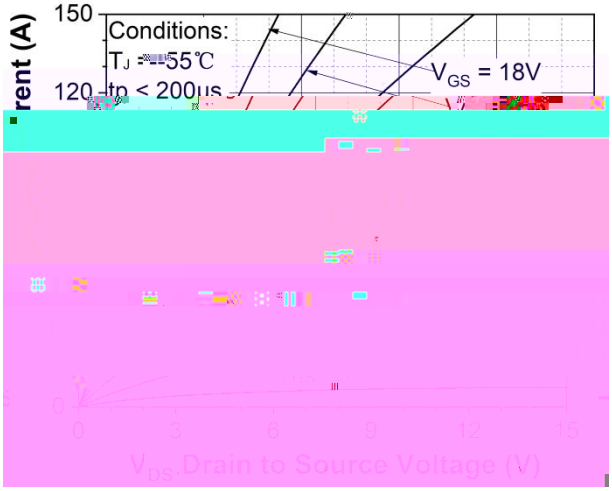


Figure 1. Output characteristics T_J = -55 ºC

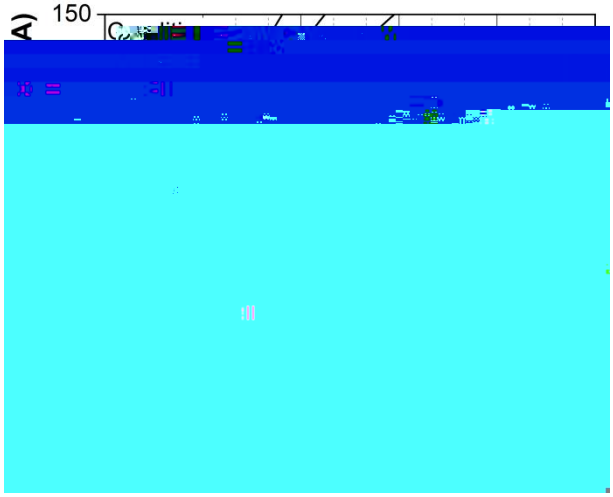


Figure 2. Output characteristics T_J = 25 ºC

Figure 3. Output characteristics T_J = 175 ºC

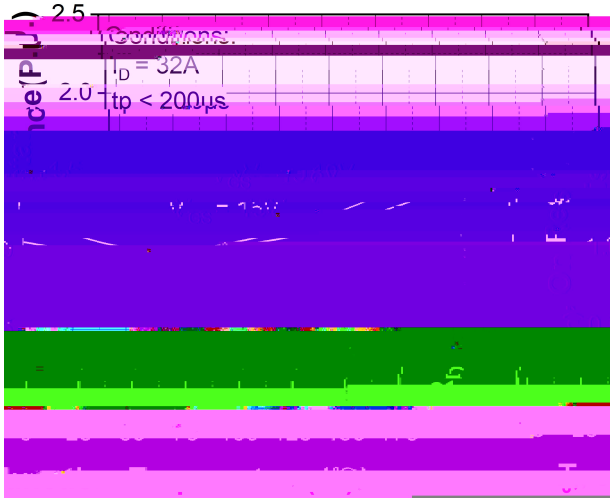


Figure 4. Normalized on-resistance vs. temperature

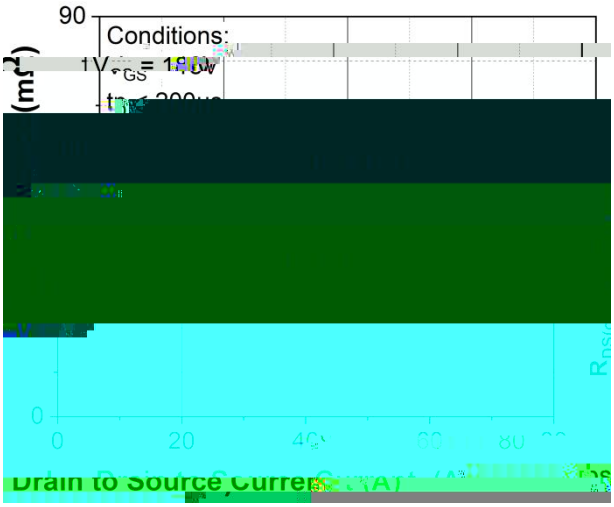


Figure 5. On-resistance vs. drain current for various temperatures

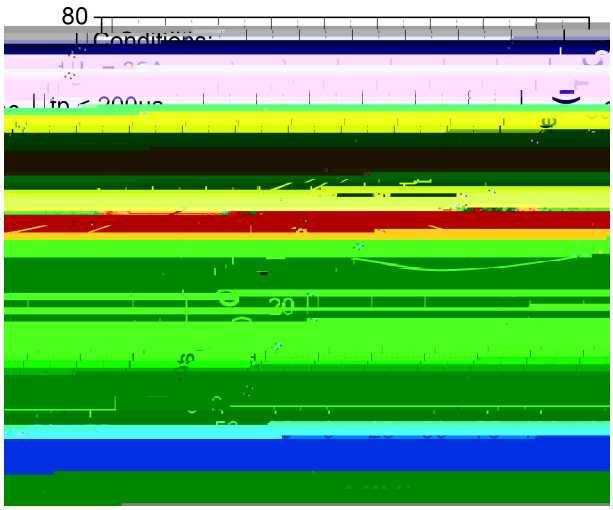


Figure 6. On-resistance vs. temperature for various gate voltages

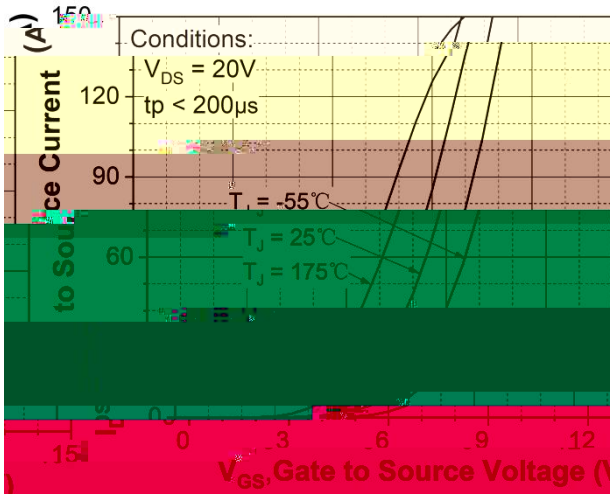


Figure 7. Transfer characteristic for various junction temperatures

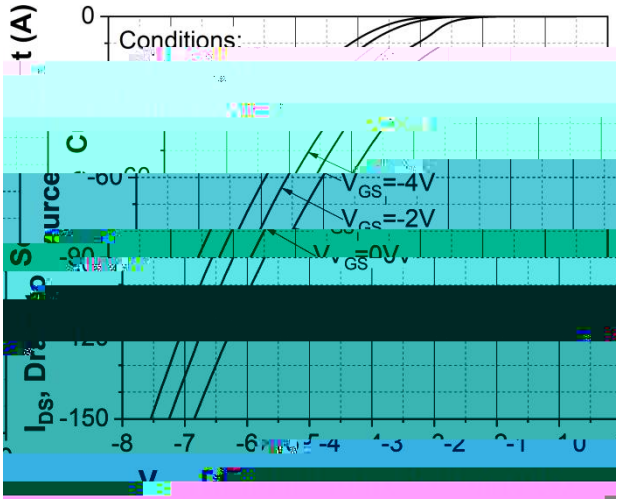


Figure 8. Body diode characteristic at T_J = -55 ºC

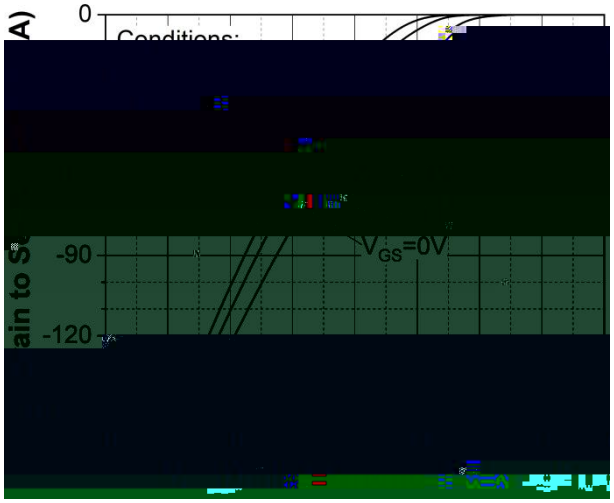


Figure 9. Body diode characteristic at T_J = 25 ºC

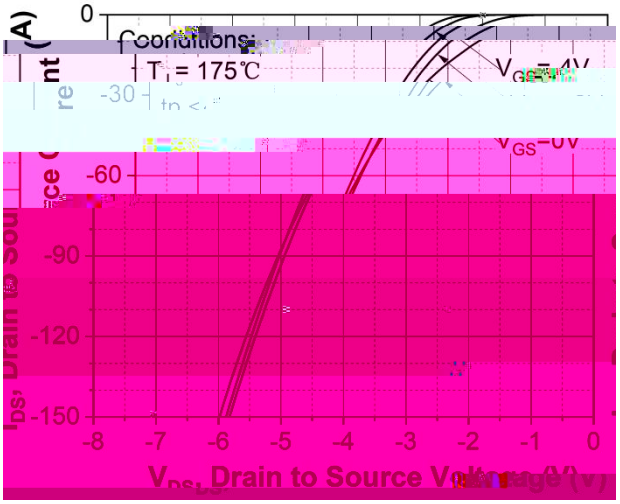


Figure 10. Body diode characteristic at T_J = 175ºC

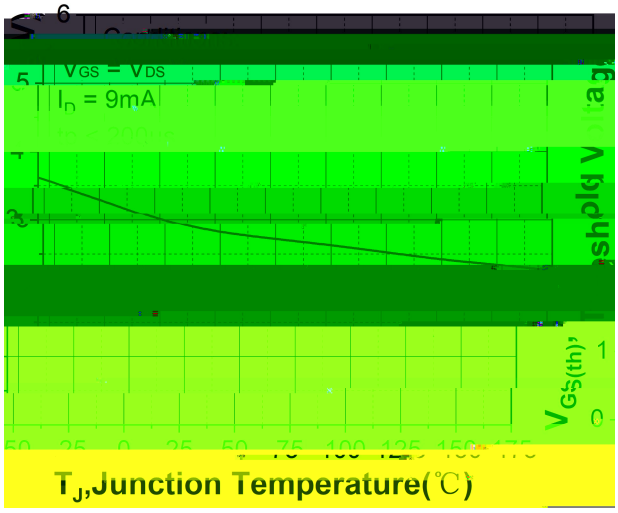


Figure 11. Threshold voltage vs. temperature

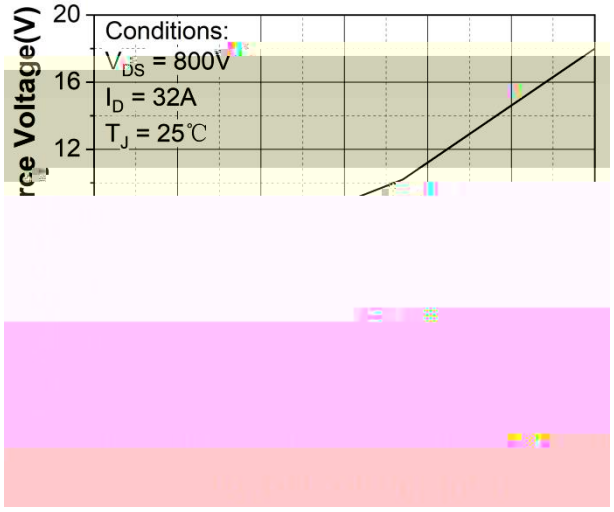


Figure 12. Gate charge characteristic

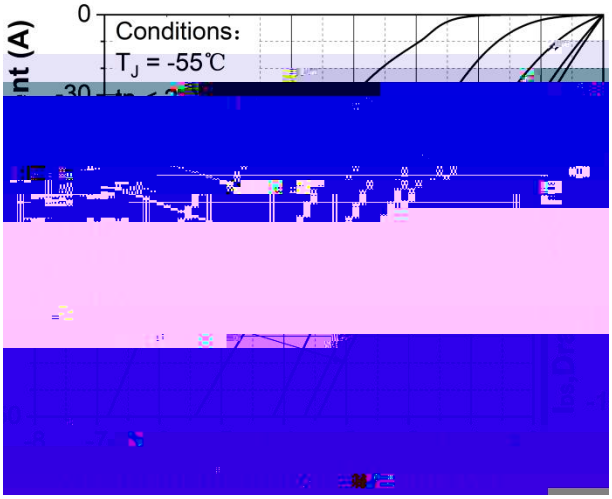


Figure 13. 3rd quadrant characteristic at T_J = -55 ºC

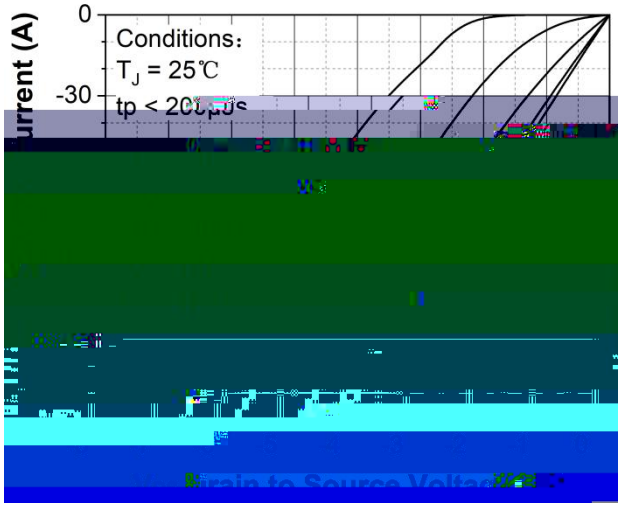


Figure 14. 3rd quadrant characteristic at T_J = 25 ºC

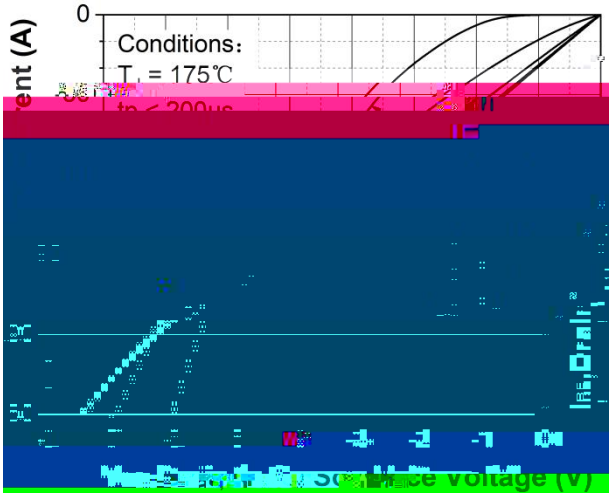


Figure 15. 3rd quadrant characteristic at T_J = 175 ºC

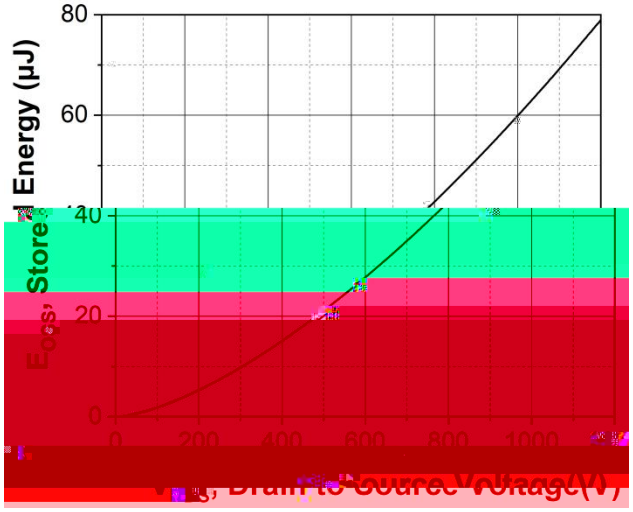


Figure 16. Output capacitor stored energy

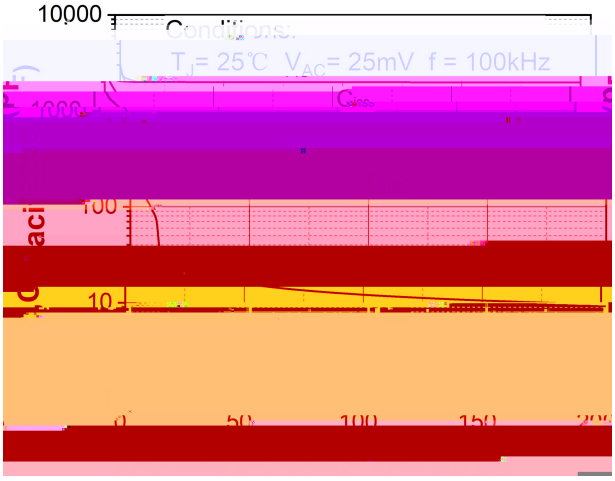


Figure 17. Capacitances vs. drain-source voltage (0 - 200V)

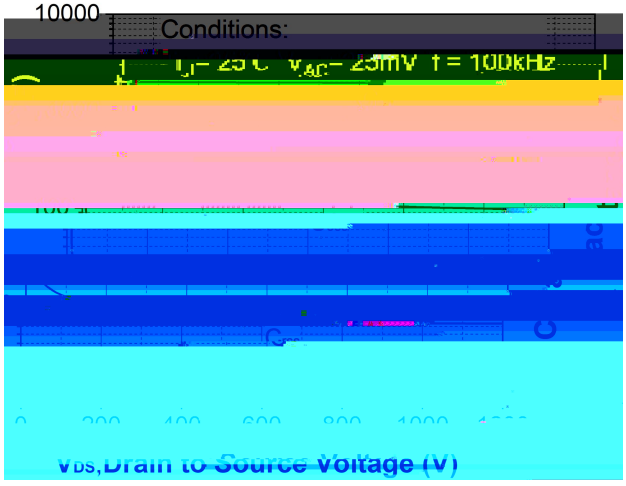
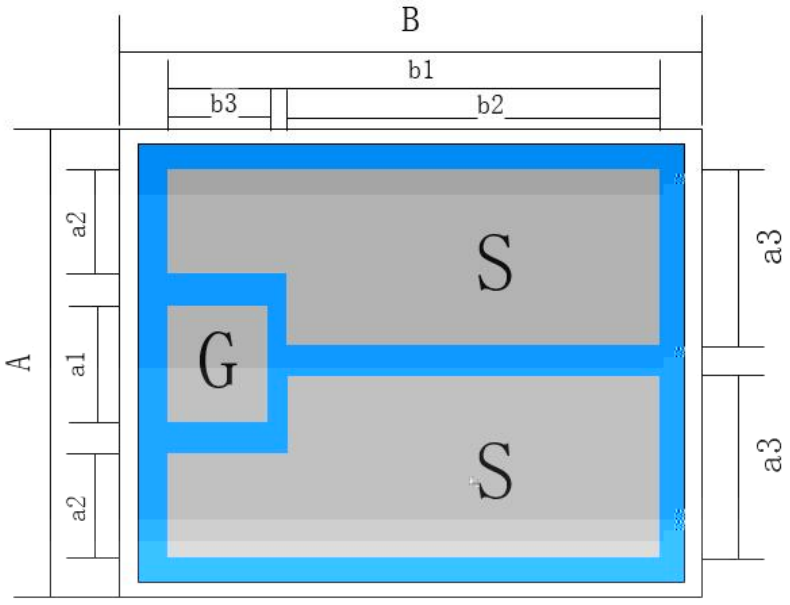


Figure 18. Capacitances vs. drain-source voltage (0 - 1200V)

Die size W x L	3.00 * 4.14	mm	
Gate pad size W x L	0.65 * 0.40	mm	
Die thickness	175	μm	
Top side source gate metallization	4	μm	Al
Back side drain metallization	1	μm	Ag



Symbol	Dimension / mm
B	4.14
b1	3.44
b2	2.89
b3	0.40
A	3.00
a1	0.65
a2	0.675
a3	1.05

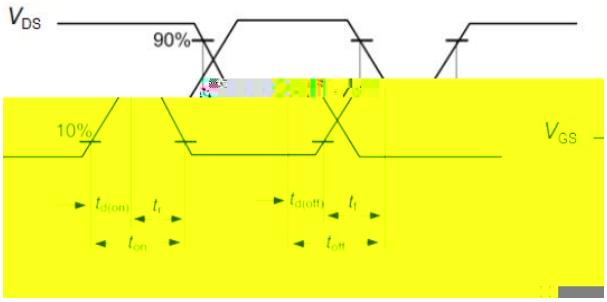


Figure A. Definition of switching times

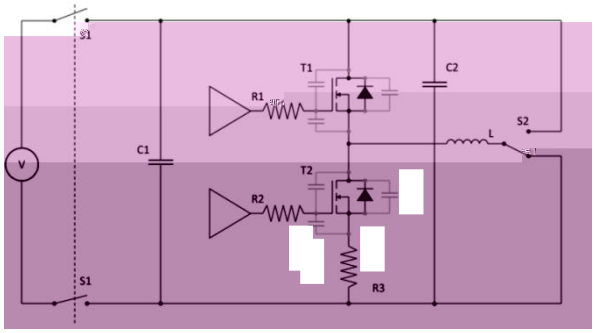


Figure B. Dynamic test circuit

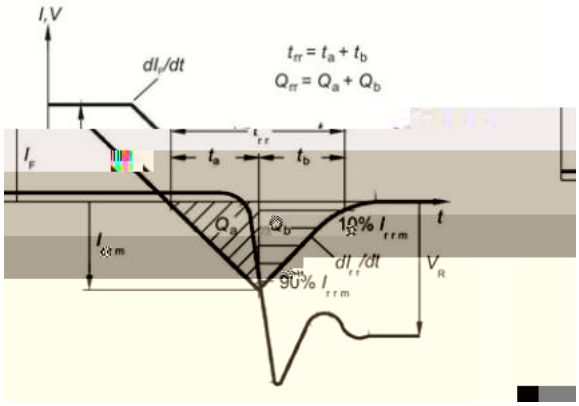


Figure C. Definition of body diode switching characteristics

7. Except as otherwise explicitly approved by Sichain in a written document signed by authorized representatives of Sichain, Sichain' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

8. For use of our products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a Sichain representatives, for example but not limited to: transportation equipment,primary communication equipment,traffic lights,fire/crime prevention, safety equipment, medical systems, and power transmission systems.